Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE)

III - SEMESTER

Sl. No.	Course Code	Course Title	Scheme of Instruction			Credits
			L	T	P	
1.	BSC 105	Mathematics – III	3	0	0	3
2.	HS 901 MB	Managerial Economics and Accountancy	3	0	0	3
3.	PC 301 EC	Electronics Devices and Circuits	3	1	0	4
4.	PC 302 EC	Digital System Design	3	1	0	4
5.	PC 303 EC	Signals and Systems	3	1	0	4
6.	PC 304 EC	Network Analysis and Synthesis	3	0	0	3
7.	MC-220	Constitution of Indian	2	0	0	0
8.	PC 351 EC	Electronics Devices and Circuits Laboratory	0	0	3	1.5
9.	PC 352 EC	Digital System Design Laboratory	0	0	3	1.5
Total			**18**	**3**	**6**	**24**

L : Lectures
T : Tutorials
P : Practical’s
CIE : Continuous Internal Evaluation
SEE : Semester End Examination
BS : Basic Sciences
ES : Engineering Sciences
PC : Professional Core
HS : Humanities and Social Sciences

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
BSC-105
Mathematics - III

Statistics, Probability, and Numerical Techniques

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

Module1: Statistical Methods

Introduction, Collection of Data, Graphical Representation, Measures of Dispersion, Moments, Skewness, Kurtosis, Correlation, Coefficient of Correlation, Lines of Regression.
(Sections 25.1, 25.2, 25.3, 25.6, 25.9, 25.10, 25.11, 25.12, 25.13, 25.14 of Text Book)

Module2: Probability & Distributions

Probability, Addition Law of Probability, Independent Events, Baye's Theorem , Random Variable, Continuous Probability Distribution, Expectation, Moment Generating Function, Binomial Distribution , Poisson Distribution, Normal Distribution, Exponential Distribution. (Sections26.1,26.4,26.5,26.6,26.7,26.9,26.10,26.11,26.14,26.15,26.16,26.19(6) of Text Book)

Module3: Numerical Techniques-I

Solution of Algebraic and Transcendental Equations, Principle of Least Squares, Method of Least Squares, Fitting of Other Curves, Finite Differences, Forward Differences, Backward Differences. (Sections 28.2, 24.4, 24.5, 24.6, 30.2, 30.2(1), 30.2(2) Of Text Book)

Module4: Numerical Techniques-II

Central Differences, Other Difference Operators, Newton's Interpolation Formulae, Gauss's Forward Interpolation Formula, Interpolation with Unequal Intervals, Numerical Differentiation. Sections 29.7, 29.4, 29.6, 29.7(1), 29.9, 30.1.of Text Book)

Module5: Numerical Techniques-III

Numerical Integration, Trapezoidal Rule, Simpson's one –third Rule, Simpson's three-eight Rule, Weddle's Rule, Solution of Simultaneous Linear Equations (Iterative Methods)
(Sections 30.4, 30.6, 30.7, 30.8, 30.10, 28.5 of Text Book)

Text Book:

B.S Grewal, Higher Engineering Mathematics, 43rd Edition, Khanna Publications.

References

1. Erwin Kreyszig, Advanced Engineering Mathematics, 8th Edition, John Wiley & Sons
2. S.C. Gupta, V.K. Kapoor, Fundamentals of Mathematical Statistics, Sultan Chand &Sons
3. S.S. Sastry, Introductory Methods of Numerical Analysis, PHI Learning Pvt. Ltd.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
HS 901 MB
MANAGERIAL ECONOMICS AND ACCOUNTANCY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

UNIT – I

Meaning and Nature of Managerial Economics: Managerial Economics and its usefulness to Engineers, Fundamental Concepts of Managerial Economics-Scarcity, Marginalism, Equimarginalism, Opportunity costs, Discounting, Time perspective, Risk and Uncertainty, Profits, Case study method.

UNIT – II

Consumer Behavior: Law of Demand, Determinants, Types of Demand; Elasticity of Demand (Price, Income and Cross-Elasticity); Demand Forecasting, Law of Supply and Concept of Equilibrium. (Theory questions and small numerical problem can be asked).

UNIT – III

Theory of Production and Markets: Production Function, Law of Variable Protection, ISO quants, Economics of Scale, Cost of Production (Types and their measurements), Concept of Opportunity cost, Concept of Revenue, Cost-Output relationship, Break-Even Analysis, Price-Output determination under perfect Competition and Monopoly (Theory and problems can be asked).

UNIT – IV

Capital Management: Significance, determination and estimation of fixed and working capital requirements, sources of capital, Introduction to capital budgeting, methods of payback and discounted cash flow methods with problems. (Theory questions and numerical problems on estimating working capital requirements and evaluation of capital budgeting opportunities can be asked).

UNIT – V

Book-keeping: Principles and significance of double entry book keeping, Journal, Subsidiary books, Ledger accounts, Trial Balance, concept and preparation of Final Accounts with sample adjustments, Analysis and interpretation of Financial statements through Ratios.
(Theory questions and numerical problems on preparation of final accounts, cash book, pretty cash book, bank reconciliations statement, calculation of some ratios).

Suggested Readings:

1. Mehta P.L., *Managerial Economics-Analysis, Problems and Cases*, Sulthan Chand & Sons Educational Publishers, 2011.
2. Maheswari S.N., *Introduction to Accountancy*, Vikas Publishing House, 2005.
3. Pnadey I.M., *Financial Management*, Vikas Publishing House, 2009.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 301 EC
ELECTRONICS DEVICES AND CIRCUITS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT –I

Semiconductor Diode: Qualitative Theory of P-N Junction, P-N Junction as a Diode, Diode Equation, Volt-Ampere Characteristics, Temperature dependence of V-I characteristic, Ideal versus Practical – Resistance levels (Static and Dynamic), Transition and Diffusion Capacitances, Diode Equivalent Circuits, Load Line Analysis, Breakdown Mechanisms in Semiconductor Diodes, Zener Diode Characteristics and Applications.

UNIT-II

Semiconductor Diode Applications: Half wave, Full wave and Bridge rectifiers – their operation, performance characteristics and analysis. Filters (L, C, LC and CLC filters) used in power supplies and their ripple factor calculations, design of Rectifiers with and without Filters.
Special Diodes (Qualitative Treatment only): Tunnel Diode, Varactor Diode, Schottky Diode, Light Emitting Diode, Photo Diode and Solar cells.

UNIT-III

Bipolar Junction Transistor: Transistor Junction formation (collector-base, base-emitter Junctions), Transistor biasing – band diagram for NPN and PNP transistors, current components and current flow in BJT, Ebers moll model, Modes of transistor operation, BJT V-I characteristics in CB, CE, CC configurations, BJT as an amplifier, BJT biasing techniques, operating point stabilization against temperature and device variations, Bias stabilization and compensation techniques, Biasing circuits design.

UNIT-IV

Small Signal Transistors equivalent circuits: Small signal low frequency h-parameter model of BJT, Approximate model, Analysis of BJT amplifiers using Approximate model for CB, CE and CC configurations; High frequency - Π model, Relationship between hybrid -Π and h – parameter model.

UNIT-V

Junction Field Effect Transistors (JFET): JFET formation, operation & current flow, V-I characteristics of JFET,

MOSFETs: Enhancement & Depletion mode MOSFETs, current equation, V-I characteristics, DC-biasing, Low frequency small signal model of FETs. Analysis of CS, CD and CG amplifiers, MOS Capacitor.

Suggested Reading:

1. Jacob Millman, Christos C. Halkias, and Satyabrata Jit, "Electronic Devices and Circuits", 3rd ed., Mc-Graw Hill Education, 2010.
2. Robert Boylestad and Louis Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Pearson India Publications, 2015.
3. Salivahanan.S, Suresh Kumar.N "Electronic Devices and circuits", 3rd edition, Tata McGraw-Hill, 2012.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 302 EC
DIGITAL SYSTEM DESIGN

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I
Number System and Logic Simplification: Number Systems, Base Conversion Methods and Complements of Numbers. Review of Boolean algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh map up to 5 variables, Tabular method.

UNIT-II
Combinational Logic Design: Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel Shifter, ALU, Comparators, Multiplexers, De-multiplexers, Encoder, Decoder, Driver & Display Devices, Code Converters.

UNIT-III
Sequential Logic Design: Building blocks like S-R, JK and Master-Slave JK Flip-flops, D and T Flip-Flops. Ripple and Synchronous Counters, Shift Registers, Finite State Machines, Design of synchronous FSM, Algorithmic State Machine charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.

UNIT-IV
Logic Families: Design of TTL Logic family, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS Logic families and their interfacing. Logic implementation using PLDs-PROM, PAL and PLA. Introduction to CPLD and FPGA.

UNIT-V
Verilog HDL: Introduction to HDL, Verilog HDL Basics: Module Concept, Lexical Conventions, Value Set, Constants, Data Types, Primitives, Module modeling styles: Structural, Data flow and Behavioral.

Suggested Reading:

1. R.P.Jain, "Modern Digital Electronics", Tata McGraw Hill, 4th Edition, 2009.
2. M.Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 4th Edition, 2012.
3. Ming-Bo Lin, "Digital System Design and Practices Using Verilog HDL and FPGAs", Wiley India Pvt. Ltd., 2012.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 303 EC
SIGNALS AND SYSTEMS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I
Introduction to Signals & Systems: Classification of signals, Operations on signals, types of systems, Exponential and Trigonometric Fourier series, Dirichlet's condition.

UNIT-II
Fourier Transform: Representation of aperiodic signal, Introduction of Fourier transform, Convergence, properties of Fourier Transform, Fourier transform of periodic signals, Singularity function, Parseval's theorem, Energy spectral density, Development of Discrete Time Fourier transform, Convergence issues associated with the DTFT.

UNIT-III
Sampling: Sampling of continuous time signals, sampling theorem, Aliasing effect, reconstruction of a signal and its samples.
Convolution & Correlation of signals: Convolution integral, Properties of convolution, Graphical method of convolution, Convolution of Discrete time signals, overlap-add and overlap-save method of discrete convolution, Definition of correlation, Auto correlation, Properties of Autocorrelation, Cross correlation of signals.

UNIT-IV
Laplace Transform: Review of Laplace transforms, region of convergence and properties, poles and zeros, relation between Laplace and Fourier transforms, properties of Laplace transform, inverse Laplace transform, Solutions to differential equation and system behavior.

UNIT-V
Z Transform: Definition of Z-Transform, Properties of Z-Transform, Region of convergence of Z-Transform, Inverse Z Transform using Inspection, Partial fraction expansion, Power series Expansion, Contour integration methods, Parseval's relation analysis of discrete time systems using Z-Transform. Realization of discrete time system using Direct form, Cascade parallel forms.

Suggested Readings:

1. Alan V. Oppenheim, Alan. S. Willsky, S Hamid Nawab, *Signals and Systems*, 2nd edition, Prentice Hall of India, 2007.
2. Lathi B.P., *Signals Systems Communications*", 1st edition, B.S. Publications, 2006.
3. Simon Haykin and Van veen, "Signal and system", Willy, second edition.

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KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 304 EC
NETWORK ANALYSIS AND SYNTHESIS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

UNIT – I

Network Theorems: Circuit Elements, Dependent and Independent Sources, Passive Elements, R, L, C, Energy Stored in L, C, Wye-Delta transformation, Nodal and Mesh analysis, Tellegen's Theorem and Maximum Power Transfer Theorem.

Network Topology: Graph, Tree, Tie set, cut set matrix, Impedance matrix formulation of node loop equations using tie-set, cut-set analysis.

UNIT – II

Two port networks: Z, Y, h, g, ABCD parameters, equivalence of two ports, Condition for Symmetry and Reciprocity. T-PI transformations, inter connection of two ports networks, Brune's test for interconnection.

UNIT – III

Response of R, L, C Networks: DC and AC excitations of RL, RC and RLC circuits, Transient Analysis. Resonance-Series and parallel. Quality factor, Bandwidth of Resonant Circuits, Steady state sinusoidal analysis using phasors, active power, reactive power and power triangle.

UNIT – IV

Filters and Attenuators and Equalizers: Constant K filters, LP, HP, BPF, BSF, m-derived composite filter design, lattice filters. Symmetrical, Asymmetric T, PI sections networks, Characteristic Impedance, Image Impedances, Iterative Impedance and propagation constant. Design of Attenuators-Symmetrical T, Pi, Lattice and Bridge-T.

UNIT – V

Network Synthesis: Fosters reactance theorems, Positive real function, Hurwitz polynomial, Driving point Impedance and admittance. Synthesis of one port RC, RL and LC networks using Foster and Cauer forms.

Suggested Readings:

1. Van Valkenberg M.E, *Network Analysis*, 3rd edition, Prentice Hall of India, 1996
2. Hayt W H, Kemerly J E Durbin, *Engineering Circuit Analysis*, 7th edition, Tata McGraw Hill, 2006.
3. Smarajit Ghosh, *Network Theory Analysis and Synthesis*, PHI Learning private Limited,2013

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
MC-220
CONSTITUTION OF INDIA

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
2	0	0	0	External Marks: 70

UNIT -1

1. Making of Indian Constitution - Constituent Assembly
2. Historical Perspective of the Constitution of India
3. Salient Features and characteristics of the Constitution of India

UNIT -2

1. The Fundamental Rights
2. The Fundamental Duties and their Legal Status
3. The Directive Principles of State Policy – Their Importance and Implementation

UNIT -3

1. Federal Structure and Distribution of Administrative, Legislative and Financial Powers between the Union and the States
2. Parliamentary Form of Government in India – The Constitutional Powers and Status of the President of India
3. Amendment of the Constitutional Provisions and Procedure

UNIT -4

1. The Judiciary
2. Constitutional and Legal Frame Work for Protection of Environmental in Global and National Level
3. Corporate Social Responsibility (CSR) International and National Scenario.

Text books:

1. D.D. Basu: An Introduction of Indian Constitution
2. Greanvile Austin: The Indian Constitution
3. Paras Diwan: Studies on Environmental cases

References books:

1. KhannnaJustice.H.R: Making of India's Constitution, Eastern Book Companies.
2. Rajani Kothari: Indian Politics
3. Ghosh Pratap Kumar: The Constitution of India. How it has been Formed, World Press.
4. A.Agrawal (Ed): Legal Control of Environmental Pollution.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 351 EC
ELECTRONICS DEVICES AND CIRCUITS LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 25
0	0	3	1.5	External Marks:50

List of Experiments

1. Measurement of static and dynamic resistances of Silicon and Germanium diodes.
2. Zener diode Characteristics and its application as voltage regulator.
3. Design, realization and performance evaluation of half wave rectifiers without and with filters.
4. Design, realization and performance evaluation of full wave rectifiers without and with filters.
5. Static characteristics of Bipolar-junction Transistor CB configuration
6. Static characteristics of Bipolar-junction Transistor CE configuration
7. Design of Self Bias Circuit
8. Drain and Transfer Characteristics of JFET
9. Design of JFET Common Source Amplifier
10. Design of Common Emitter BJT amplifier
11. Characteristics of UJT
12. Simulate any two experiments using PSPICE

Note: A minimum of 10 experiments should be performed

Suggested Reading:

1. Paul B. Zbar, Albert P. Malvino, *Micheal A. Miller*, *Basic Electronics*, *A text – Lab Manual*, 7th Edition, TMH 2001.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 302 EC
DIGITAL SYSTEM DESIGN LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 25
0	0	3	1.5	External Marks: 30

List of Experiments

1. Implementation of all logic gates using universal gates
2. Implementation of half adder, full adder, half Subtractor and full Subtractor using universal gates
3. Implementation Boolean functions using suitable multiplexer
4. Design a 4 – bit Adder / Subtractor
5. Design and realization a 4 – bit gray to Binary and Binary to Gray Converter
6. Truth table verification of SR Flip Flop using NAND and NOR gates.
7. Truth table verification of JK, D and T flip flops
8. Shift register implementation using flip flops
9. Synchronous counter implementation using flip flops
10. Truth table verification of asynchronous counters
11. Design of Up/Down counters
12. Realization of logic gates using DTL, TTL, ECL, etc.,

Note: A minimum of 10 experiments should be performed.

Suggested Reading:

1. M.Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 4th Edition, 2012.

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B. Tech. (ECE)

IV - SEMESTER

Sl. No.	Course Code	Course Title	Scheme of Instruction			Credits
			L	T	P	
1	PC 401 EC	Analog Electronic Circuits	3	1	0	4
2	PC 402 EC	Stochastic Processes	3	0	0	3
3	PC 403 EC	Electromagnetic Waves and Transmission Lines	3	1	0	4
4	PC 404 EC	Pulse and Integrated Circuits	3	1	0	4
5	PC 405 EC	Computer Architecture and Organization	4	0	0	4
6	ES 401 EI	Electronic Measurements and Instrumentation.	3	0	0	3
7	MC 210	Environmental Science	2	0	0	0
8	PC 451 EC	Analog Electronic Circuits Laboratory	0	0	3	1.5
9	PC 452 EC	Pulse and Integrated Circuits Laboratory	0	0	3	1.5
Total			**21**	**3**	**6**	**25**

L : Lectures
T : Tutorials
P : Practical's
CIE : Continuous Internal Evaluation
SEE : Semester End Examination
BS : Basic Sciences
PC : Professional Core
PW : Project Work

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-401 EC
ANALOG ELECTRONIC CIRCUITS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I

Small Signal Amplifiers: Introduction to Hybrid-π model, relationship between hybrid-π & h-parameter model; Classification of amplifiers, mid-frequency, Low-frequency and high frequency analysis of single and multistage RC coupled amplifier with BJT and FET. Analysis of transformer coupled amplifier in mid frequency, Low frequency and high frequency regions with BJT.

UNIT-II

Feedback Amplifiers Analysis and Design: The feedback concept, General characteristics of negative feedback amplifier, Effect of negative feedback on input and output impedances, Voltage and current, series and shunt feedbacks. Stability considerations, Local Versus global feedback.

UNIT-III

Oscillators Analysis and Design: Positive feedback and conditions for sinusoidal oscillations, RC oscillators, LC oscillators, Crystal oscillator, Amplitude and frequency stability of oscillator.
Regulators: Transistorized series and shunt regulators.

UNIT-IV

Large Signal Amplifiers: BJT as large signal audio amplifiers, Classes of operation, Harmonic distortion, power dissipation, efficiency calculations. Design considerations of transformer coupled and transform less push-pull audio power amplifiers under Class-A. Class-B, Class D and Class-AB operations.

UNIT-V

RF Voltage Amplifiers: General consideration, Analysis and design of single tuned and double tuned amplifiers with BJT, Selectivity, gain and bandwidth. Comparison of multistage, single tuned amplifiers and double tuned amplifiers. The problem of stability in RF amplifiers, neutralization & uni-laterisation, introduction to staggered tuned amplifiers.

Suggested Reading:

1. Jacob Millman, Christos C. Halkias, and Satyabrata Jit, Electronic Devices and Circuits, 3rd ed., McGraw Hill Education, 2010.
2. David A. Bell, Electronic Devices and Circuits, 5th ed., Oxford University Press, 2009.
3. S Salivahanan, N Kumar, and A Vallavaraj, Electronic Devices and Circuits, 2nd ed., McGraw Hill Education, 2007.
4. Jacob Millman, Christos Halkias, Chetan Parikh, Integrated Electronics, 2nd ed., McGraw Hill Education (India) Private Limited, 2011.
5. Donald L Schilling & Charles Belove, Electronics Circuits, Discrete & Integrated, 3rd ed., McGraw Hill Education (India) Private Limited, 2002.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-402 EC
STOCHASTIC PROCESSES

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

Unit-I

Introduction to Stochastic Processes (SPs): Definition and examples of SPs, classification of random processes according to state space and parameter space, types of SPs, elementary problems

Unit-II

Discrete-time Markov Chains (MCs): Definition and examples of MCs, transition probability matrix, Chapman-Kolmogorov equations; calculation of nstep transition probabilities, limiting probabilities, classification of states, ergodicity, stationary distribution, transient MC; random walk and gambler's ruin problem, applications.
Continuous-time Markov Chains (MCs): Kolmogorov - Feller differential equations, infinitesimal generator, Poisson process, birth-death process, Applications to queueing theory, inventory analysis, communication networks, finance and biology.

Unit-III

Branching Processes: Definition and examples branching processes, probability generating function, mean and variance, Galton-Watson branching process, probability of extinction.
Renewal Processes: Renewal function and its properties, elementary and key r e n e w a l theorems, cost/rewards associated with renewals, Markov renewal and regenerative processes, 4 applications.
Stationary Processes: Weakly stationary and strongly stationary processes, moving average and auto regressive processes.

Unit-IV

Martingales: Conditional expectations, definition and examples of martingales, inequality, convergence and smoothing properties, applications in finance

Text/Reference Books:

1. G. R. Grimmett and D. R.Stirzaker, Probability and Random Processes, 3rd Edition, Oxford University Press, 2001.
2. S.M. Ross, Stochastic Processes, 2nd Edition, Wiley, 1996 (WSE Edition).
3. J. Medhi, Stochastic Processes, 3rd Edition, New Age International, 2009.
4. H.M. Taylor and S.Karlin, An Introduction to Stochastic Modeling, 3rd Edition, Academic Press, New York, 1998.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-403 EC
ELECTROMAGNETIC THEORY AND TRANSMISSION LINES

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I

Electrostatics: Review of Vector Calculus and Coordinate systems and Transformation, Coulomb's Law, Electric Field Intensity, Electric field due to different charge distributions - Electric Field due to Line Charge, Sheet Charge and Volume Charge Distribution. Electric Flux, Flux Density, Gauss's Law and Applications. Energy and Potential, Potential Field of a Point Charge, System of Charges, potential gradient, Energy density in Electrostatic fields, Electric Dipole, convection and conduction currents, continuity equation and relaxation time, Poisson's and Laplace's Equations, Capacitance and Capacitors.

UNIT-II

Magnetostatics: Biot-Savart Law, Ampere's Circuital Law, Applications of Ampere's Law, Magnetic Flux Density, Magnetic Scalar and Vector Potentials, Forces due to magnetic fields, Magnetic Dipole, Magnetization, Inductors and Inductances, Magnetic Energy.

UNIT-III

Time Varying Fields and Maxwell's Equations: Faraday's Law, Transformer and Motional EMF's, Displace Current, Maxwell's Equations in Differential and Integral Forms, Time-Varying Potentials, Electromagnetic Boundary Conditions, Time-Harmonic Fields.

UNIT-IV

EM Wave Propagation: Uniform Plane Wave, Wave Propagation in Free Space, Dielectrics, Good Conductors-Skin Effect. Poynting's Theorem and Wave Power, Poynting Vector, Instantaneous, average and complex pointing vector, Wave Polarization-Linear, Circular and Elliptical polarizations, Reflection of Uniform Plane Waves at Normal incidence and Oblique incidence angles, Reflection coefficient, Transmission coefficient, power and energy calculations.

UNIT-V

Transmission Lines: Circuit representation, Equations of voltage and current on transmission line, propagation constant and characteristic impedance, Lossless Line, Distortion less Line, Infinite line concepts, Input impedance relations of open and short-circuited transmission lines, reflection coefficient and VSWR. The Smith Chart, Transmission Line Impedance Matching-Impedance Matching by Quarter wave Transformer, Single Stub Matching and Double Stub Matching.

Suggested Readings:

1. Matthew N,O. Sadiku, *Principles of Electromagnetics*, Oxford University Press, 2009, 4th edition.
2. David K.Cheng, *Field and Wave Electromagnetics*, Pearson Education, 2001, 2nd edition.
3. W.H.Hayt,Jr. and J.A Buck, *Engineering Electromagnetics*, Tata McGraw-Hill, 2006, 7th edition.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-404 EC
PULSE AND INTEGRATED CIRCUITS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT- I

Linear Wave Shaping: High pass, low pass RC circuits, their response for sinusoidal, step, pulse and ramp inputs. RC network as differentiator and integrator, attenuators, its applications in CRO probe.

Non-Linear Wave Shaping: Diode clippers, Transistor clippers, clipping at two independent levels. Clamping operation and Clamping circuit theorem.

UNIT-II

Differential amplifiers: Classification, DC and AC Analysis of Single/Dual input Balanced and Unbalanced output configurations using BJTs. Level Translator.

Operational Amplifier: OP AMP Block diagram, ideal Op-amp characteristics, features, parameters and their Measurement, Input and Output Offset voltages and currents, Slew rate, CMRR, PSRR, Frequency response and Compensation Techniques.

UNIT-III

OPAMP Applications: Inverting and Non-inverting Amplifiers, Integrator and differentiator, summing amplifier, precision rectifier. Active filters: Low pass, high pass, band pass and band stop.

UNIT-IV

Digital Logic families: characteristics of digital ICs, RTL, TTL family IC's, characteristics and comparison among various series of TTL Family IC's, ECL family-operation and characteristics, CMOS logic family, comparison among CMOS series, Interfacing TTL and CMOS IC's.

UNIT-V

555 Timers: Functional Diagram, Monostable, Astable and Schmitt Trigger Applications.

Voltage regulators: Fixed and variable voltage regulators (78XX and 79XX).

Data Converters: Digital-to-analog converters (DAC): Weighted resistor, inverted R-2R ladder, Analog-to-digital converters (ADC): dual slope, successive approximation, flash type. Specifications of Data Converters.

Suggested Reading:

1. J. Millman and H. Taub, Pulse, Digital and Switching Waveforms - McGraw-Hill, 1991.
2. David A. Bell, Solid State Pulse circuits - PHI, 4th Edn., 2002.
3. J.V. Wait, L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory and applications, McGraw Hill, 1992.
4. D.Roy Chowdhury, Shail B.Jain, “Linear Integrated Circuits”, 4/e, New / Age International (P) Ltd., 2008.
5. Ramakanth A Gayakwad, -Op-Amps and Linear Integrated Circuits‖, 3rd Edition, Prentice-Hall of India Limited, New Delhi, 1995.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-405 EC
COMPUTER ARCHITECTURE AND ORGANIZATION

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
4	0	0	4	External Marks: 70

UNIT-I
CPU Organization: Common bus structure, Arithmetic, Logic and Shift Unit using multiplexer, Register, Instructions, Design of CPU. Example: Intel 8085 – Programming model, Addressing modes, overview of Instruction set, Design of flowchart for CPU operation.

UNIT-II
Data Path Design: Fixed-Point Arithmetic: Addition, Subtraction, Multiplication -Robertson's, Booth's algorithms, Array Multiplier and Wallace tree multiplication, Division - Restoring and Non-restoring algorithms, floating point arithmetic and BCD Adder, Shifter: Barrel shifter and Logarithmic shifter, Examples: HDL descriptions of Fixed-Point and Floating-Point arithmetic.

UNIT-III
Control Design: Basic concepts, Hardwired Control unit design approach: classical and one-hot methods, Micro-programmed Control unit approach: basic concept, micro-program sequencer, Design examples: control unit designs for GCD processor, DMA controller and CPU control unit.

UNIT-IV
Memory and System Organization: Memory Organization: Memory hierarchy, Main memory: RAM, ROM, DRAM, Multi-level memory, cache memory: principles, address mapping techniques, replacement policies, System Organization: communication methods, IO and system control: Programmed IO, DMA and interrupts and Input-Output Processor (IOP), Examples: Three-level cache hierarchy in Intel Pentium Processor.

UNIT-V
Advances in Computer Organization: Reduced Instruction Set Computer (RISC): characteristics and architecture, Parallel processing: Pipeline – Arithmetic and Instruction, Pipeline Conflicts, Instruction Level Parallelism: super-pipeline, super-scalar architectures.

Suggested Reading:

1. Morris Mano M, *Computer System Architecture*, 3rd edition, Prentice Hall India, 2007.
2. William Stallings, *Computer Organization and Architecture, Design for Performance*, 7th edition, Prentice Hall India, 2006.
3. John P. Hayes, *Computer Architecture and Organization*, 3rd edition, McGraw Hill, 1998.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
ES 401 EI
ELECTRONIC MEASUREMENTS & INSTRUMENTATION

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

UNIT- I

Electronic Measurements: Physical measurement, forms and methods of measurements, measurement errors, Statistical analysis of measurement data, Probability of errors, Limiting errors, Standards, Definition of standard units. International standards, primary standards, secondary standards, IEEE Standards, Testing and calibration

Voltage and current measurements: DC & AC voltage measurements using Rectifier, Thermocouple & Electronic voltmeters, Ohm meter, Digital Voltmeters, Range Extension of Ammeters & Voltmeter, Digital Multi meter Frequency Counters, Frequency synthesizer, Wave meters, Wave Analyzers, Output Power meter.

UNIT-II

Bridges: AC Bridges – measurement of inductance: - Maxwell‘s bridge, Anderson bridge, Hays Bridge measurement of capacitance:-Schering bridge, measurement of impedance: – Kelvin‘s bridge, Wheat Stone bridge, HF bridges, problems of shielding, and grounding, Q-meter.

UNIT-III

Oscilloscopes: CRO operation, CRT characteristics, probes, Time base sweep modes, Trigger generator, Vertical amplifier, modes of operation, A, B, alternate & chop modes, sampling oscilloscopes, storage oscilloscope, Standard specifications of CRO, Synchronous selector circuits. Analyzers Spectrum analyzers, Different types of spectrum analyzers, Display Devices and Display Systems, Logic Analyzers – State & time referenced data capture. Scalar and Vector network analyzers.

UNIT-IV

Transducers: Transducer & its classification – Basic Requirements of Transducer – Resistive Transducers: Potentiometric type, Strain Gauge type; Capacitive Transducers: Variable gap type, Variable area type and Variable Dielectric type – Inductive Transducers: Variable Reluctance type and LVDT type – Piezo Electric Transducer: Piezoelectric effect, Piezoelectric materials, PZT - Photo electric Transducers: LDR, Photo diode and Photo transistor

UNIT- V

Transducer Applications: Force Measurement using Strain Gauge transducer – Temperature measurement using RTD & Thermocouple type transducer - Pressure measurement using Differential Capacitive type transducer – Acceleration Measurement using Piezoelectric Accelerometer - Flow Measurement using Electro Magnetic Flow Meter – Fluid Velocity Measurement using Hot wire Anemometer – Level Measurement using Ultrasonic Level Gauge – Sound Level Meter – Data Acquisition system

TEXT BOOKS

1. Electronic Instrumentation – HS Kalsi, Tata McGraw Hill, 2004.
2. Electronic Instrumentation and measurements techniques by Helfrick and W.D. Cooper, PHI publications.

REFERENCE BOOKS

1. Principles of measurement systems, John P. Bentley: 3rd edition, Addison Wesley Longman, 2000.
2. Measuring Systems, Application and Design: E. O. Doebelin, McGraw Hill.
3. Electrical and Electronic Measurements: Sawhney, Khanna Publ.
4. Electronic Instrumentation and measurements: David A. Bell, 2nd Edition, PHI, 2003.
5. Electronic instruments and instrumentation Technology, M.M.S. Anand: Prentice Hall of India, 2004

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
MC-210
ENVIRONMENTAL SCIENCE

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
2	0	0	0	External Marks: 70

UNIT-I

Environmental studies: Definition, scope and importance, need for public awareness. Natural resources: Water resources use and exploitation of Surface and Ground water. Floods, Drought, Cconflicts over water, Dams-merits and demerits.

Land Resources: Land as a resource, Effects of modern Agriculture, Fertilizer-pesticide problems, Water logging and Salinity, land degradation, soil erosion and Desertification.

Energy resources: Growing energy needs renewable and non-renewable energy resources.

UNIT-II

Ecosystems and Biodiversity: Concept of Ecosystem, structure and function of an ecosystem, producers, consumers and decomposers, energy flow in ecosystem, food chains, food web, ecological pyramids, aquatic ecosystem (ponds, lakes, streams, rivers, oceans, estuaries) **Biodiversity:** Genetic species and ecosystem diversity, bio-geographical classification of India. Value of biodiversity, threats to biodiversity, endangered and endemic species of India, conservation of biodiversity.

UNIT-III

Environmental Pollution: Causes, effects and control measures of air pollution, water pollution, soil pollution, noise pollution, Thermal pollution. Solid waste management, Municipal solid waste management, Biomedical waste management and, hazardous waste management.

Disaster management: Types of disasters, impact of disasters on environment, infrastructure, and development.

UNIT-IV

Environmental protection and Global issues: Environmental protection acts: Air, Water, Forest and wild life Acts, enforcement of Environmental legislation. Water conservation, watershed management, and Eenvironmental ethics. Climate change, Global warming, acid rain, ozone layer depletion.

UNIT-V

Sustainable future: Concept of Sustainable Development, Sustainable development goals, Population and its explosion, Crazy Consumerism, Urban Sprawl, Environmental Education, Human health, Environmental Ethics, Concept of Green Building, Ecological Foot Print, Life Cycle assessment (LCA), Low carbon life style.

Suggested Readings:

1. De A.K., "*Environmental Chemistry"*, Wiley Eastern Ltd., 1989.
2. Odum E.P., "*Fundamentals of Ecology"*, W.B. Sunders Co., USA,1975.
3. G.L. Karia and R.A. Christian, *Waste Water Treatment, Concepts and Design Approach,* Prentice Hall of India, 2005.
4. Benny Joseph, *Environmental Studies,* Tata McGraw Hill,2005.
5. V.K.Sharma, *Disaster Management, National Centre for Disaster Management,* IIPE, Delhi,1999.
6. *Environmental Science: towards a sustainable future* by Richard T. Wright. 2008 PHL Learning Private Ltd. New Delhi

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-451 EC
ANALOG ELECTRONIC CIRCUITS LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
0	0	3	1.5	External Marks: 70

List of Experiments

1. Two Stage RC Coupled CE BJT amplifier.
2. Two Stage RC Coupled CS FET amplifier.
3. Voltage Series Feedback Amplifier.
4. Voltage Shunt Feedback Amplifier.
5. Current series feedback Amplifier
6. RC Phase Shift Oscillator.
7. Hartley & Colpitt's Oscillators
8. Design of Class A and Class B Power amplifiers.
9. Constant-k low pass & high pass filters.
10. m-Derived low pass & high pass filters.
11. Series and Shunt voltage Regulators
12. RF Tuned Amplifier

SPICE:

13. Two Stage RC Coupled CS FET amplifier.
14. Voltage Series Feedback Amplifier
15. Current Shunt Feedback Amplifier

Suggested Reading:

1. Paul B. Zbar, Albert P. Malvino, *Micheal A. Miller, Basic Electronics, A text – Lab Manual*, 7th Edition, TMH 2001.

Note: A minimum of 10 experiments should be performed. It is mandatory to simulate any three experiments using SPICE

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) IV SEMISTER
PC-452 EC
PULSE AND INTEGRATED CIRCUITS LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
0	0	3	1.5	External Marks: 70

List of Experiments

1. Verification of Low Pass circuit response to step, pulse and square inputs
2. Verification of High Pass RC Circuit response to step, pulse and square inputs
3. Design and verification of RC integrator and differentiator Circuits
4. Design and verification of Low pass and High pass Filters
5. Design and verification of Clipping Circuit (shunt and series)
6. Design and verification of Clamping Circuits (Positive and Negative, with and without bias)
7. Measurement of OPAMP Parameters
8. Inverting and Non-inverting OP-AMP Voltage follower
9. Integrator and Differentiator using OPAMP
10. Design and verification of Active filters
11. Astable and Mono stable multi vibrator using NE555 IC
12. Voltage regulators
13. Digital to Analog Converters
14. Analog to Digital Converters

Note: A minimum of 10 experiments should be performed.

Suggested Reading:

1. Robert Boylestad and Louis Nashelsky, “Electronic Devices and Circuit Theory”, 5th Edition, Prentice-Hall of India Private Limited, New Delhi, 1995.
2. David A. Bell, Laboratory Manual for “Electronic Devices and Circuits”, 4th Edition, Prentice-Hall of India Private Limited, New Delhi, 2004.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

S. No.	Course Code	Course Title	Scheme of Instruction			Lecture hrs/week	Scheme of Examination		Credits
			L	T	P		CIE	SEE	
1	PC3101EC	Control System Engineering	3	0	0	3	30	70	3
2	PC3102EC	Analog and Digital Communication	4	0	0	4	30	70	4
3	PC3103EC	Microprocessor and Microcontroller	4	0	0	4	30	70	4
4	PC3104EC	Antenna Wave Propagation	3	0	0	3	30	70	3
5	PE-I*	Program Elective –I	3	0	0	3	30	70	3
6	HS3108LW	Law and Engineering	2	0	0	2	30	70	2
8	PC3109EC	Analog and Digital Communication Laboratory	0	0	3	3	25	50	1.5
9	PC3110EC	Microprocessor and Microcontroller Laboratory	0	0	3	3	25	50	1.5
10	PW3111EC	Mini-project	0	0	4	4	50	00	2
	Total		**19**	**0**	**10**	**29**	**280**	**520**	**24**

***(PE-I) Professional Elective – I**
PE3105EC: Digital System Design using Verilog HDL
PE3106EC: Bio-Medical Electronics.
PE3107EC: MOOCS Course**

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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PC3101EC CONTROL SYSTEM ENGINEERING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT – I

Introduction to control systems: Basic components, classification of control systems, effects of feedback, mathematical modeling of physical systems, transfer functions, DC and AC position control systems, block diagrams, signal flow graphs.

UNIT – II

State-variable analysis of continuous data systems: state, state variables, state equations, solution of state equations, state transition matrix and its properties, state diagram, relationship between state equations and transfer functions, concept and testing of controllability and observability.

UNIT – III

Time-domain analysis: Typical test signals, steady-state error, unit-step response and time-domain specifications and transient response of a prototype second-order system.

Stability analysis of continuous data systems: Bounded-Input, Bounded-output stability, Zero input and asymptotic stability, Routh-Hurwitz criterion.

Root-Locus technique: Properties and construction of the root loci.

UNIT – IV

Frequency-domain analysis: frequency response and frequency domain specifications, Nyquist stability criterion, Bode plots, relative stability – gain margin and phase margin.

UNIT – V

Design of control systems: Cascade and feedback compensation using Bode plots. Phase lag, phase lead and phase Lag-Lead compensators and their design.

Controllers: Introduction to PI, PD and PID controllers.

Suggested Readings:

1. Benjamin C. Kuo, "*Automatic Control Systems"*, Prentice Hall of India, 2009, 7th Edition.
2. I.J.Nagrath and M Gopal, "*Control System Engineering"*, New Age International Private Limited, New Delhi, 2008, 5th Edition
3. Katsuhiko Ogata, "*Modern Control Engineering*", Prentice-Hall of India Private Limited, New Delhi, 2003, 4th Edition.

Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PC3102EC ANALOG AND DIGITAL COMMUNICATION

Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT- I

Modulation Schemes: Introduction to communication system, Need for modulation, TDM and FDM, Amplitude Modulation, Frequency Modulation (FM) and Phase Modulation (PM), concept of Generation and demodulation of the above.

UNIT- II

Transmitters and Receivers: classification of transmitters, AM and FM radio transmitters and Receivers. Noise performance of AM, FM and PM systems: Sources of noise, thermal noise, shot noise, noise in linear systems, Signal-to noise ratio (SNR) calculations for DSB-SC AM, SSB, FM and PM systems.

UNIT-III

Analog Pulse Modulation Schemes: Sampling of continuous-time signals, pulse amplitude modulation (PAM), pulse width modulation (PWM) and pulse position modulation (PPM), generation and demodulation.

Digital Coding Techniques: Elements of digital communication system, sampling theorem, quantization noise, source coding techniques: PCM, DPCM, DM, noise in PCM, DM system. Performance comparison of above systems.

UNIT – IV

Error Control Coding: Binary discrete channels, types of transmission errors, need for error control coding, Coding theory: Introduction, source coding/decoding, Huffman coding, Shannon fano coding, linear block codes, binary cyclic codes, characteristics of BCH codes, convolution codes.

UNIT – V

Digital Carrier Modulation Techniques: optimum receiver, coherent and non-coherent ASK, FSK, PSK, DPSK, MSK, and QPSK schemes, M-ary signaling schemes, and synchronization methods.

Spread Spectrum Modulation: introduction, generation and characteristics of PN sequences. DSSS, FHSS system and their application, acquisition scheme for spread spectrum receivers, tracking of FH and DS signals.

Suggested Readings:

1. Simon Haykin, *"Communication Systems"*, 4th Edition, John WiLey&sons.inc, 2000.
2. K Sam Shanmugam, *"Digital and Analog Communication Systems"*, John Wiley & sons, 1979.
3. Herbert Taub and Donald L.Schilling, *"Principles of Communication Systems"*, 2nd Edition,Tata McGraw-Hill publishing company Limited, New Delhi, 1986.
4. George Kennedy, Bernard Davis, *"Electronic Communication Systems"*, 4th Edition, Tata McGraw-Hill publishing company Limited, New Delhi, 1993.
5. John G.Proakis, *"Digital Communications"*, 4th Edition, Tata McGraw- Hill publishing company Limited, New Delhi, 2003.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PC3103EC MICROPROCESSOR AND MICROCONTROLLER

Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*

CIE: 30 marks *SEE: 70 marks*

UNIT – I

Introduction to 8086: The 8086 Microprocessor Family- Overview, 8086 architecture, segmented memory, Pin configuration, Maximum and Minimum mode of operation, addressing modes, Memory read and write bus cycles, memory interfacing,

UNIT – II

Assembly Language Programming: Instructions for data transfer, arithmetic, logical, simple sequence program Jumps, Flags, and Conditional jumps, Loops and Constructs, Instruction Timing and Delay Loops; String instructions, Procedures and Macros, Assembler Directives, Interrupts in 8086.

UNIT – III

Peripherals: Programmable Peripheral Interface 8255 – examples using DAC, ADC, stepper motor etc., DMA controllers, Programmable Interrupt Controller 8259, Programmable Interval Timer 8254, USART 8251.

UNIT – IV

Introduction to microcontroller: Difference between microcontroller and microprocessor, 8051microcontroller architecture. 8051 registers. Memory organizations-program memory and data memory, internal RAM and bit addressable memory, special function registers.

UNIT - V

8051 assembly language programming: instruction sets, addressing modes, programming using different instructions, timers, I/O Ports, interrupts, Serial ports. Interfacing 8051 with peripherals – LCD, Stepper motor, ADC, DAC, PWM, and Relay.

Suggested Readings:

1. Douglas V.Hall, *"Microprocessors and Interfacing Programming and Hardware"*, 2nd Edition, Tata McGraw- Hill publishing company Limited, New Delhi, 1994.
2. Walter A.Triebel and Avatar singh, *"The 8088 and 8086 Microprocessors Programming, Interfacing,Software, Hardware and Applications"*, Prentice-Hall of India Private Limited, New Delhi, 1996.
3. Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin D.McKinlay, *"The 8051 Microcontroller and Embedded Systems using Assembly and C"*, 2nd Edition, Pearson education, 2009.

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PC3104EC ANTENNA WAVE PROPAGATION

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT - I

Fundamentals of Antenna theory: Principle of radiation, Basic Antenna Parameters – Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity, Gain, Antenna Apertures, Effective Height, Illustrative Problems. Retarded Potentials – Helmholtz Theorem Thin Linear Wire Antennas – Radiation from Small Electric Dipole, Quarter Wave Monopole and Half Wave Dipole – Current Distributions, near field and far field Components, Radiated Power, Radiation Resistance, Beam Width, Directivity, Effective Area and Effective Height. Loop Antennas – Introduction, Small Loop, Comparison of Far Fields of Small Loop and Short Dipole.

UNIT - II

Antenna Arrays: Basic two element array, N element uniform linear array, Pattern multiplication, Broadside and End fire array, Planar array, Concept of Phased arrays, Adaptive array, Basic principle of antenna Synthesis- Binomial array, Tschebyscheff array.

UNIT - III

Practical Antennas: Yagi-uda antenna, V- Antenna, Rhombic antenna, Travelling wave antennas, Microstrip antennas – Introduction, Features, Advantages and Limitations, Rectangular Patch Antennas – Geometry, Design equations and Characteristics.

UNIT - IV

Aperture and Modern Antennas: - Reflector Antennas – Introduction, Flat Sheet and Corner Reflectors, Paraboloidal Reflectors – Geometry, Pattern Characteristics, Feed Methods, and Reflector Types – Related Features, Illustrative Problems. Horn Antennas – Types, Fermat's Principle, Radiation from sectorial and pyramidal horns, Design Considerations of Pyramidal Horns, Reconfigurable antenna, Active antenna, Dielectric antennas, Electronic band gap structure and applications

UNIT - V

Wave propagation: Ground wave propagation. Space and surface waves, Tropospheric refraction and reflection. Sky wave propagation – Virtual height, critical frequency, Maximum usable frequency – Skip distance, Fading, Multi hop propagation

Suggested Reading:

1. Constantine A. Balanis, "*Modern Antenna Handbook*", a John Wiley & Sons, Inc., Publication, 2008.
2. John D.Kraus, Ronald J.Marhefka and Ahmed S.Khan, "*Antennas for All Applications*" 3rd Edition, Tata McGraw- Hill publishing company Limited, New Delhi, 2006.
3. K.D.Prasad, "*Antennas and Wave Propagation*", Khanna or Satya Publications.

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PROFESSIONAL ELECTIVE –I

PE3105EC DIGITAL SYSTEM DESIGN USING VERILOG HDL

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT – I
Structural modeling: Overview of Digital Design with Verilog HDL, modules and ports, gate-level modeling and design examples.
Dataflow modeling: dataflow modeling, operands and operators. Switch Level Modeling: CMOS switches and bidirectional switches and design examples. Introduction to test bench design.

UNIT – II
Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, multi-way branching, Loops, Sequential and Parallel blocks, Generate blocks. Combinational, sequential logic modules and design examples.

UNIT-III
Digital Integrated Circuits: Classification of Integrated Circuits, Comparison of Various Logic Families Combinational Logic ICs – Specifications and Applications of TTL-74XX & Code Converters, Decoders, De-multiplexers, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, De-multiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor and Magnitude Comparators.

UNIT-IV
Sequential Logic IC's and Memories: Familiarity with commonly available TTL 74XX, CMOS 40XX Series ICs – All Types of Flip-flops, Asynchronous and synchronous Counters, Decade Counters, Shift Registers. Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture and applications, Static & Dynamic RAMs.

UNIT –V
Real time implementations: Fixed-Point Arithmetic modules: Addition, Multiplication, Division, Arithmetic and Logic Unit (ALU), Timer, Universal Asynchronous Receiver and Transmitter (UART), DSP modules: FIR and IIR filters, CPU design: Data path and control units.

Suggested Readings:

1. Samir Palnitkar, *"Verilog HDL A Guide to Digital Design and Synthesis,"* 2nd Edition, Pearson Education, 2006.
2. R.P.Jain, *"Modern Digital Electronics"*, Tata McGraw Hill, 4th Edition, 2009.
3. Ming-Bo Lin, *"Digital System Designs and Practices: Using Verilog HDL and FPGA*," Wiley India Edition, 2008.
4. J. Bhasker, *"A Verilog HDL Primer,"* 2nd Edition, BS Publications, 2001.

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B. Tech. (ECE) V SEMESTER

PROFESSIONAL ELECTIVE –I

PE3106EC BIO-MEDICAL ELECTRONICS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I
Block diagram of a medical instrumentation system, Challenges faced with physiological measurements, Role of electronic circuits in analysis of biomedical signals. Bio-potential electrodes: Electrode-Electrolyte Interface, Equivalent circuit and applications of biopotential electrodes.

UNIT-II
Electrocardiography: Block diagram and preamplifier circuit, Single channel & multi-channel ECG systems, Holter monitors, Blood Pressure measurement: components and working principle of sphygmomanometer, Direct and indirect methods of Blood Pressure measurements. Electromagnetic and Ultrasonic techniques of Blood flow measurement.

UNIT-III
Phonocardiography- Origin of Heart Sounds, types of microphones for heart sound measurement, Contact and non-contact type of measurement. Electroencephalography: EEG-Block diagram and preamplifier circuit, electrodes and their placement. Lead configuration and general EEG graphs. Evoked potentials and their measurement.

UNIT-IV
Electromyography: Introduction to EMG signals, EMG-Block diagram and circuits, Electrodes and their placement, Nerve conduction velocity determination using EMG. Oximeters-Ear, pulse, skin reflectance.

UNIT-V
Impedance plethysmography. Ultrasonic, Xray and nuclear imaging. Prostheses and aids: pacemakers, defibrillators, heart-lung machine, artificial kidney, aids for the handicapped.

Suggested Readings:

1. Webster J.G., Medical Instrumentation Application and Design. Houghton Mifflin, 2009.
2. Khandpur R.S. Hand Book of Biomedical Instrumentation, Tata McGrawHill,2003.
3. John Enderle, Susan M. Blanchard, and Joseph Bronzino, Introduction to Biomedical Engineering, Second Edition, 2005.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

HS3108LW LAW AND ENGINEERING

Credits: 2

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

Unit-I: The Legal System - Meaning, nature and definition of jurisprudence - Schools of jurisprudence- Analytical, Historical, Philosophical and Sociological Schools of jurisprudence - Meaning and Definition of Law - The Nature and functions of Law - Sources of Law - Legal and Historical sources – Precedent/Case Law as Source of Law - Definition of Precedent, Kinds of Precedent - Legislation as Source of Law- Definition of Legislation - Classification of Legislation – Supreme and Subordinate Legislation – Court System and Hierarchy of Judiciary in India - Concept of Alternative Dispute Resolution System (ADR) – History and Reasons for the growth of ADR – Important forms of ADR – Mediation - Negotiation – Arbitration - Definition of Arbitration and Essentials - Online Dispute Resolution (ODR)**.**

Unit-II: Society and Constitutional law - Social Change: Definition, nature and characteristics of Social change – Social Transformation - Factors of Social Change - Law and social Change - State, Law and Society, their inter-relationship and interdependence - Identification of Goals of Social Changes in Indian Constitution - Constitution-Meaning and Significance - Nature and Salient Features of Indian Constitution - Preamble to Indian Constitution – Fundamental Rights - Right to Equality(Art.14-18) – Freedoms and Restrictions under Art.19 - Right to Life and Personal Liberty - Directive Principles of State Policy – Significance – Nature – Classification.

Unit-III: Contract law - Definition and essentials of a Valid Contract - Meaning and Definition of Consideration - Capacity of the parties to enter into contract - Concepts of Free Consent - Lawful Object - Illegal agreements - Void and Voidable contracts - Discharge of Contracts - Remedies for breach of contract - Kinds of damages - Contract of sale of Goods – Formation of contract of sale - Sale and Agreement to Sell -Conditions and Warranties - Express and implied Conditions and Warranties - Caveat Emptor - Rights and duties of seller and buyer before and after sale – Rights of Unpaid Seller - Remedies of breach.

Unit-IV: Business Organizations - Corporate Personality - General Principles of Company Law – Companies Act, 2013 - Nature and Definition of Company - Characteristics of a Company - Different kinds of Company - Private Company and Public Company – Registration & Incorporation of Company –Advantages and Disadvantages of Incorporation - Lifting of the Corporate Veil – Company distinguished from Partnership and Limited Liability Partnership - Shares & Stock - Kinds of shares – Share Capital - Directors – Different kinds of Directors - Appointment, position , qualifications and disqualifications - Powers of Directors - Rights and Duties of Directors – Corporate Governance and Role of Directors – Meetings of Company - Winding up of Companies-Modes of Winding up of Companies.

Unit-V: Meaning, Definition and Concept of Environment - Types of Environment - Concept of Pollution – Sources of Pollution, Types of Pollution, and Effects of Pollution – Ozone Depletion – Global Warming – Climate Change - The Environment Protection Act of 1986 - Main Aims and Objectives of the Act - Meaning, Nature, Classification and significance of Intellectual Property - The main forms of Intellectual Property - Patents - Concept of Patent - Kinds of Patents - The Patents Act, 1970 - Rights and obligations of a patentee - The notion of 'abuse' of patent rights - Infringement of patent rights and remedies available - Meaning, Definition and Nature of Cyber crimes - Information Technology Act, 2000 - Specific Cyber crimes - Cyber Stalking – Hacking - Child Pornography - Phishing – Cyber Crimes and Issues of Privacy - Investigation and Jurisdiction over Cyber crimes.

References:

1. Salmond: Jurisprudence, Universal Publishers.
2. Mahajan V.D.: Legal Theory and Jurisprudence, Eastern Book Company, Lucknow.
3. M.P.Jain, Indian Constitutional Law, Wadhwa & Co, Nagpur
4. H.M.Seervai, Constitutional Law of India (in 3 Volumes), N.M.Tripathi, Bombay
5. J.N.Pandey, Constitutional Law of India, Central Law Agency, Allahabad
6. Anson: Law of Contract, Clarendon Press, Oxford, 1998.
7. Avtar Singh: Law of Contract , Eastern Book Company, Lucknow, 1998.
8. P.S.Atiyah: Sale of Goods Act, Universal Book Traders, Delhi.
9. Acharya N.K.: Law relating to Arbitration and ADR, Asia Law House, Hyderabad
10. Tripathi S.C.: Arbitration, Conciliation and ADR, Central Law Agency, Allahabad.
11. Avatar Singh: Arbitration and Conciliation, Eastern Law Book House, Lucknow
12. V.K. Krishna Iyer: Environment Pollution and Law
13. Paras Diwan : Environmental Law and Policy in India,1991
14. Dr. N. Maheshwara Swamy, Environmental Law, Asia Law House, Hyderabad.
15. Avtar Sing : Company Law, Eastern Book Company.
16. Ramaiah: Company Law, Wadhwa & Co.
17. P. Narayanan: Patent Law, Eastern Law House, 1995.
18. Roy Chowdhary, S.K. & Other: Law of Trademark, Copyrights, Patents and Designs, Kamal Law House, 1999.
19. Dr. G.B. Reddy, Intellectual Property Rights and the Law Gogia Law Agency.
20. Dr Jyoti Rattan, Dr Vijay Rattan, Cyber Laws & Information Technology, 2019, Bharat Law House, New Delhi

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) V SEMESTER

PC3109EC ANALOG AND DIGITAL COMMUNICATION LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 25 marks *SEE: 50 marks*

List of experiments

Cycle-I

1. AM generation and Demodulation
2. FM generation and Demodulation
3. Spectrum Analyzer and Analysis of AM and FM Signals
4. Radio Receiver measurements
5. AGC Characteristics of Radio Receiver
6. Squelch Circuit and Frequency Multiplier Circuit
7. Pre-emphasis and De-emphasis Circuits

Cycle-II

8. Sampling and Reconstruction of Sine Wave
9. PAM generation and Demodulation
10. PWM generation and Demodulation
11. PPM generation and Demodulation
12. PCM generation and Demodulation
13. Delta Modulation
14. Spectrum Analyzer and Analysis of PAM and PWM Signals
15. ASK, FSK, PSK, QPSK and DPSK modulation and Demodulation using MATLAB

Note: At least 10 experiments need to be completed in a semester (5 from analog and 5 from digital communication systems).

Suggested Readings:

1. Simon Haykin, *"Communication Systems"*, 4th Edition, John Wiley &sons.inc, 2000.
2. George Kennedy, Bernard Davis, *"Electronic Communication Systems"*, 4th Edition, Tata McGraw-Hill publishing company Limited, New Delhi, 1993.
3. K.C. Raveendranathan *"Communication systems Modelling and simulation using Matlab and Simulink"* Universities Press 2011.

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B. Tech. (ECE) V SEMESTER

PC3110EC MICROPROCESSOR AND MICROCONTROLLER LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 25 marks *SEE: 50 marks*

List of Experiments:

1. Addition, subtraction using 8085
2. Multiplication and division using 8085
3. Simple programs on 8086 kits
4. Searching and sorting using 8086 assembly language
5. String operations like concatenation and swapping using 8086
6. DAC interface to 8086
7. ADC interface to 8086
8. Stepper motor interface to 8086
9. Study of Keil software for 8051
10. Basic programs using 8051 instructions
11. Flashing LED program using 8051
12. Timer program to generate square wave on ports of 8051

Suggested Readings:

1. Ramesh S.Gaonkar, *"Microprocessor Architecture programming and Applications with the 8085"*, 5th Edition, Penram International publishing (India) private Limited, 1999.
2. Douglas V.Hall, *"Microprocessors and Interfacing programming and Hardware"*, 2nd Edition, Tata McGraw- Hill publishing company Limited, New Delhi, 1994.
3. Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin D.McKinlay, *"The 8051 Microcontroller and Embedded Systems using Assembly and C*", 2nd Edition, Pearson education, 2009.

Annexure

**Student is required to complete MOOCs course offered by the following agencies. The student is required to take prior approval from the Department, before registering for any course. The student can register for such a course in 5th Semester and/or 6th semester. Unless the student submits a pass certificate, he/she shall not be eligible for the award of degree.

SWAYAM: www.swayam.gov.in ,NPTEL: www.onlinecourse.nptel.ac.in

Abbreviations

L	:	Lectures	T	:	Tutorials
P	:	Practicals	CIE	:	Continuous Internal Evaluation
SEE	:	Semester End Examination	PC	:	Professional Core

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S. No.	Course Code	Course Title	Scheme of Instruction			Lecture hrs/week	Scheme of Examination		Credits
			L	T	P		CIE	SEE	
1	PC3201EC	Digital Signal Processing	4	0	0	4	30	70	4
2	PC3202EC	VLSI Design	4	0	0	4	30	70	4
3	PC3203EC	Data Communication and Computer Networks	3	0	0	3	30	70	3
4	PE-II*	Professional Elective–II	3	0	0	3	30	70	3
5	PE-III**	Professional Elective–III	3	0	0	3	30	70	3
6	OE-I#	Open Elective-I	3	0	0	3	30	70	3
8	PC3214EC	Digital Signal Processing Laboratory	0	0	3	3	25	50	1.5
9	PC3215EC	Electronic Design and Automation Laboratory	0	0	3	3	25	50	1.5
10	PW3216EC	Summer Internship***	6-weeks				-	-	-
	Total		**20**	**0**	**6**	**26**	**230**	**520**	**23**

***(PE-II) Professional Elective–II**
PE3204EC: Embedded System Design
PE3205EC: Artificial Neural Networks and Fuzzy Logic
PE3206EC: Adaptive Filter Theory and Applications
PE3207EC: Optical Communication

****(PE-III) Professional Elective–III**
PE3208EC: Information theory and Coding
PE3209EC: Wireless Communications
PE3210EC: Radar Engineering
PE3211EC: MOOCs Course

 # Please Refer Annexure

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B. Tech. (ECE) VI SEMESTER

PC3201EC DIGITAL SIGNAL PROCESSING

Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I
Introduction: Review of Discrete Time Fourier Transform, Concept of frequency in continuous and discrete time signals, DFT and its properties, linear convolution, circular convolution. Computational complexity of direct Computation of DFT, Fast Fourier Transform, DIT and DIF, FFT algorithms for RADIX-2 case, in-place computation, Bit reversal, Finite word length effects in FFT algorithms, Use of FFT in Linear Filtering.

UNIT-II
FIR Filters: FIR digital filter design techniques. Properties of FIR digital filters, design of FIR filters using windows and frequency sampling techniques, linear phase characteristics. Realization diagrams for IIR and FIR filters, finite word length effects.

UNIT-III
IIR Filters: Analog filter design – Butterworth and Chebyshev approximations, IIR digital filter design techniques, impulse invariant technique. Bilinear transform technique. Comparison of FIR and IIR filters, frequency transformations.

UNIT- IV
Multirate signal processing: Introduction, decimation by a factor D, interpolation by a factor I, sampling rate conversion by a rational factor I/D, design of practical sampling rate converter, S/W implementation of sampling rate converter, application of Multirate signal processing.

UNIT-V
DSP Processors: Introduction to Fixed point Digital Signal Processors, TMS 320C54XX processor-architecture, addressing modes, instruction set, Assembly programming, programming issues, Applications of DSP processors.

Suggested Readings:

1. John G.Proakis and Dimitris G. Manolakis, *"Digital Signal Processing principles, Algorithms and Applications"*, 3rd Edition, Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Alan V. Oppenheim and Ronald W. Schafer," Discrete *Time Signal Processing*", 3rd edition, Prentice Hall, Upper Saddle River, NJ,2010
3. Sanjit K. Mitra, "*Digital Signal Processing: A Computer-Based Approach*", 4/e, McGraw-Hill, New York,2011
4. Avatar sing and S.Srinivasan, *"Digital Signal Processing implementation using DSP Microprocessors with Examples from TMS320C54XX"*, Thomson Books Icole, 2004.

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B. Tech. (ECE) VI SEMESTER

PC3202ECVLSI DESIGN
Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT – I
Design Abstraction in Digital circuits, Fabrication process flow of nMOS and pMOS transistors, Overview of CMOS and BiCMOS technologies, MOSFET Transistor under static conditions, channel Length Modulation, Velocity Saturation, Sub-threshold Condition, Threshold variations, MOS structure Capacitance, CMOS Latch up, Technology scaling.

UNIT – II
CMOS Inverter, Voltage Transfer Characteristics, Static Power Consumption, Dynamic Power Consumption, Propagation Delay, Power-Energy and Energy-Delay Product, Layout Design of basic gates, Silicon on Insulation Technology, FinFET, Comparison of SOI and FinFET.

UNIT – III
Designing Combinational Logic gates in CMOS: Complementary CMOS, Ratioed Logic, Pass Transistor Logic, Dynamic CMOS logic-basic principle, Signal integrity issues in Dynamic Design, domino logic, np-CMOS logic, Merits and Demerits of above logic styles. Designing sequential logic: Bistability Principle, Multiplexer based latch, Dynamic latch, Pipelining.

UNIT – IV
Designing Arithmetic Building Blocks: Adder, Binary Adder, Full Adder, and Mirror Adder, Transmission gate-based Adder, Manchester Carry Chain Adder, Carry Bypass Adder, Carry Look ahead Adder, Carry Save Adder, Multiplier, Carry Save Multiplier, Barrel Shifter, and Logarithmic Shifter. Design of Memory Structures: ROM cells, PROM, EPROM, EEPROM, Flash Memory, SDRAM and DRAM.

UNIT – V
Implementation of strategies for Digital ICs, Testing of VLSI circuits: VLSI Chip Yield, Test procedures; Design for Testability- Ad Hoc Testing, Scan Based testing, Boundary Scan Design, Built in Self-Test, Built-in logic block observer, Test Pattern Generator, Automatic Test Pattern Generation (ATPG).

Suggested Readings:

1. JAN.M. Rabaey, A. Chandrakasan and B. Nikholic, *"Digital Integrated Circuits – A Design Perspective"*, 2nd Edition, PHI, 2007.
2. David A Hodges, H. Jackson and R. A. Saleh, *"Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology"*, 3rd Edition, Tata McGraw Hill, 2007.
3. John. P. Uymera, *"Introduction to VLSI Circuits and system"*, student edition, John Wiley and Sons, 2003.

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B. Tech. (ECE) VI SEMESTER

PC3203ECDATA COMMUNICATION AND COMPUTER NETWORKS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT - I

Data communication: A Communication Model, The Need for Protocol Architecture and Standardization, Network Types: LAN, WAN, MAN. Network Topologies: Bus, Star, Ring, Hybrid. Line configurations. Reference Models: OSI,TCP/IP.
Circuit switching: Circuit Switching Principles andconcepts.
Packet switching: Virtual circuit and Datagram subnets, X.25.

UNIT - II

Data Link Layer: Need for Data Link Control, Design issues, Framing, Error Detection and Correction, Flow control Protocols: Stop and Wait, Sliding Window, ARQ Protocols, HDLC. **MAC Sub Layer:** Multiple Access Protocols: ALOHA, CSMA, Wireless LAN. IEEE 802.2, 802.3, 802.4, 802.11, 802.15, 802.16 standards. Bridges and Routers.

UNIT - III

Network Layer: Network layer Services, Routing algorithms: Shortest Path Routing, Flooding, Hierarchical routing, Broadcast, Multicast, Distance Vector Routing, and Congestion Control Algorithms.
Internet Working: The Network Layer in Internet: IPV4, IPV6, Comparison of IPV4 and IPV6, IP Addressing, ATMNetworks.

UNIT - IV

Transport Layer: Transport Services, Elements of Transport Layer, Connection management, TCP and UDP protocols, ATM AAL Layer Protocol.

UNIT - V

Application Layer: Domain Name System, SNMP, Electronic Mail, World Wide Web. **Network Security:** Cryptography Symmetric Key and Public Key algorithms, Digital Signatures, Authentication Protocols.

Suggested Reading:

1. Andrew S Tanenbaum, *"Computer Networks,"* 5/e, Pearson Education,2011.
2. Behrouz A. Forouzan, *"Data Communication and Networking,"*3/e, TMH,2008.
3. William Stallings, *"Data and Computer Communications,"* 8/e, PHI,2004.
4. Douglas EComer, *"Computer Networks and Internet"*, Pearson Education Asia,2000.
5. PrakashC. Gupta, *"Data Communications and Computer Networks"*, PHI learning,2013

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE–II

PE3204EC EMBEDDED SYSTEM DESIGN

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT-I

Introduction to Embedded Systems: The Embedded Design Life Cycle - Product Specification, Hardware/Software Partitioning, Iteration and Implementation, Detailed Hardware (selection of processor) and Software Design, Hardware/Software Integration, Product Testing and Release, Maintenance and Upgradation.

UNIT-II

ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, ARM processor fundamentals, registers, current program status register, pipeline, exceptions, interrupts, and vector table, core extensions, architecture revisions, ARM processor families.

UNIT-III

Embedded processing with ARM CORTEX on Zynq: Fundamentals of FPGA, types of FPGA, case study of Xilinx FPGA, Processing System, programmable logic, programmable logic interfaces, security, Zynq 7000 family members, Zynq versus standard FPGA, Zynq versus standard processor.

UNIT-IV

Embedded Software Development Tools: Host and Target Machines, Cross Compilers, Cross Assemblers, Tool Chains, Linkers/Locators for Embedded Software, Address Resolution, Locator Maps. Getting Embedded Software into Target System: PROM programmer, ROM emulator, In Circuit- Emulators, Monitors, Testing on Your Host Machine - Instruction Set Simulators, Logic Analyzers.

UNIT-V

Introduction to Real Time Operating Systems: Tasks and task states, tasks and Data, Semaphores and shared data. Operating system services: Message queues, mailboxes and pipes, timer functions, events, memory management, Interrupt routines in an RTOS environment.

Suggested Readings:

1. Arnold S Berger, "*Embedded Systems Design*", South Asian edition, CMP Books, 2005.
2. Andrew Sloss, Dominic Symes, Chris Wright, *"ARM System Developer's Guide: Designing and Optimizing System Software"*, Elsevier, 2004.
3. Louise H Crockett, Ross.A.Elliot et *al " The Zynq Book*" , Edition 1, Strathclyde academic media, July 2014.
4. David E Simon, *"An Embedded software primer"*, Pearson, 2012

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

Unit –I

Introduction to Neural Networks: Introduction, Biological Neuron, Biological and Artificial Neuron Models, Characteristics of ANN, McCulloch-Pitts Model, Essentials of Artificial Neural Networks: Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Applications of ANN.

Unit- II

Feed Forward Neural Networks: Single Layer: Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.
Multilayer: Generalized Delta Rule, Derivation of Back propagation (BP) Training, Summary of Back propagation Algorithm, Kolmogorov Theorem

Unit–III

Associative Memories: Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory, Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem Architecture of Hopfield Network: Discrete and Continuous versions

Unit- IV

Classical & Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

Unit - V

Logic System Components: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods. Fuzzy logic applications

Suggested Readings:

1. James A Freeman and Davis Skapura, *"Neural Networks"*, Pearson Education, 2002.
2. B. Yeganaranarana, "*Artificial Neural Networks*", Prentice Hall, New Delhi, 2007.
3. Bart Kosko, "*Neural Networks and Fuzzy Logic System*", PHI Publications.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ADAPTIVE FILTER THEORY AND APPLICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT - I

Approaches to the development of adaptive filter theory. Introduction to filtering, smoothing and prediction. Wiener filter theory, introduction; Error performance surface; Normal equation; Principle of orthogonality; Minimum mean squared error; example.

UNIT - II

Gradient algorithms; Learning curves; LMS gradient algorithm; LMS stochastic gradient algorithms; convergence of LMS algorithms.

UNIT - III

Applications of adaptive filter to adaptive noise cancelling, Echo cancellation in telephone circuits and adaptive beam forming.

UNIT - IV

Kalman Filter theory; Introduction; recursive minimum mean square estimation for scalar random variables; statement of the kalman filtering problem: the innovations process; Estimation of state using the innovations process; Filtering examples.

UNIT V

Vector Kalman filter formulation. Examples. Application of kalman filter to target tracking.

Suggested Reading:

1. Sophoclas, J. Orphanidies, *"Optimum signal processing an introduction"*, McMillan, 1985.
2. Simon Haykins, *"Adaptive signal processing"*, PHI, 1986.
3. Bernard Widrow, *"Adaptive signal processing"*, PHI, 1986.
4. Bozic. SM., *"Digital and Kalman Filtering"*.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3207EC OPTICAL COMMUNICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT -I
Overview of Optical Fiber Communication: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, basic optical laws, Ray theory, step index and graded index fibers, ray optics representation, fiber materials.

UNIT - II
Transmission Characteristics of Optical Fibers: Introduction, Attenuation, absorption, scattering losses, bending loss, dispersion, Intra modal dispersion, Inter modal dispersion.

UNIT - III
Optical Sources and Detectors: Introduction, LED's, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors.

UNIT - IV
Fiber Couplers and Connectors: Introduction, fiber alignment and joint loss, fiber splices, fiber connectors and fiber couplers.
Optical Receiver: Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection.

UNIT –V
Analog and Digital Links: Analog links – Introduction, overview of analog links, CNR, Digital links – Introduction, point–to–point links, System considerations, link power budget, resistive budget.
WDM Concepts and Components: WDM concepts, overview of WDM operation principles, WDM standards,

Suggested Reading:
1. Optical Fiber Communication – Gerd Keiser, 4th Ed., MGH, 2008.
2. Optical Fiber Communications– – John M. Senior, Pearson Education, 2007.
3. Fiber optic communication – Joseph C Palais: 4th Edition, Pearson Education.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –III

PE3208EC INFORMATION THEORY AND CODING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT - I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies. Channel Coding Channel capacity, binary symmetric channel, binary erasure channel, Shannon's channel coding theorem, Huffman coding.

UNIT - II

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - III

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT - IV

Convolutional Codes: Encoding of Convolutional Codes- Structural and Distance Properties, state, tree, trellis diagrams, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT - V

BCH Codes: Minimum distance and BCH bounds, Decoding procedure for BCH codes, Syndrome computation and iterative algorithms, Error locations polynomials for single and double error correction.

Suggested Readings:

1. K. Sam Shanmugam, "*Digital and analog communication systems*", John Wiley India Pvt. Ltd, 1996.
2. Simon Haykin, "*Digital communication*", John Wiley India Pvt. Ltd, 2008.
3. Muralidhar Kulkarni, K.S. Shivaprakasha, "*Information Theory and Coding*", Wiley India Pvt. Ltd, 2015, ISBN: 978-81-265-5305-1.
4. Shu Lin, Daniel J. Costello, Jr, "*Error Control Coding- Fundamentals and Applications*", Prentice Hall, Inc 2014.
5. Man Young Rhee, "*Error Correcting Coding Theory*" McGraw – Hill Publishing 1989

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –III

PE3209EC WIRELESS COMMUNICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I

Overview of wireless communication system, History of wireless communication, current wireless systems, wireless spectrum, 2G, 3G, 4G and 5G wireless communication standards.

UNIT-II (Qualitative treatment only)

Comparison of digital Modulation schemes: Information Capacity, Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Band Width Efficiency.

UNIT-III

The wireless communication environment, classification of fading channels, different parameters related to fading mechanisms, modeling of wireless systems, system model for narrowband signals, Rayleigh fading wireless channel.

UNIT-IV

Basics mechanism of Code division multiple access (CDMA), fundamentals of CDMA codes, Introduction to MIMO wireless communication systems, MIMO system model, MIMO zero forcing and MMSE receiver.

UNIT-V

Multi carrier modulation, data transmission using multiple carriers, basics of orthogonal frequency division multiplexing (OFDM) systems, cyclic prefix, MIMO-OFDM system

Suggested Readings:

1. A. K. Jagannatham, *Principles of modern wireless communications systems*. McGraw Hill Education, 2015.
2. A. Goldsmith, *Wireless Communications*. New York: Cambridge Univ. Press, 2005.
3. T. S. Rappaprt, Wireless communications principles & Practices, Pearson, 2010.

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PROFESSIONAL ELECTIVE –III

PE3210EC RADAR ENGINEERING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I

Basics of Radar: Introduction, Maximum Unambiguous Range, Simple form of Radar Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications, Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation.

UNIT-II

CW and Frequency Modulated Radar: Doppler Effect, CW Radar – Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar, Illustrative Problems.FM-CW Radar, Range and Doppler Measurement, Block Diagram and Characteristics (Approaching/ Receding Targets), FM-CW altimeter, Multiple Frequency CW Radar.

UNIT-III

MTI and Pulse Doppler Radar: Introduction, Principle, MTI Radar with – Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancellers – Filter Characteristics, Blind Speeds, Double Cancellation, And Staggered PRFs. Range Gated Doppler Filters, MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler radar.

UNIT-IV

Tracking Radar: Tracking with Radar, Sequential Lobing, Conical Scan, Monopulse Tracking Radar –Amplitude Comparison Monopulse (one- and two- coordinates), Phase Comparison Monopulse, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers.

UNIT-V

Detection of Radar Signals in Noise: Introduction, Matched Filter Receiver – Response Characteristics and Derivation, Correlation Function and Cross-correlation Receiver, Radar Receivers: Noise Figure and Noise Temperature, Displays – types. Duplexers – Branch type and Balanced type, Introduction to Phased Array Antennas.

Suggested Readings:

1. Introduction to Radar Systems – Merrill I. Skolnik, TMH Special Indian Edition, 2nd Edition, 2007.
2. Introduction to Radar Systems – Merrill I. Skolnik, 3rd Edition, Tata McGraw-Hill, 2001.
3. Radar Principals, Technology, Applications – Byron Edde, Pearson Education, 2004.
4. Radar Principles – Peebles, Jr., P.Z.Wiley, NewYork, 1998.

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B. Tech. (ECE) VI SEMESTER

PC3214ECDIGITAL SIGNAL PROCESSING LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE:3 hours*
CIE: 25 Marks *SEE: 50 Marks*

List of Experiments

1. (a)Generation of basic signals based on recursive difference equations.
   (b) Operations on Basic sequences
2. (a) Linear and Circular Convolutions in time domain and frequency domain
   (b) Determination of autocorrelation and Power Spectrum of a given signal(s)
3. (a) Fast Fourier Transform – DIT and DIF algorithm
   (b) Spectrum analysis using DFT
4. (a) Generation of windows – Rectangular, Hamming and Hamming window
   (b) Design of LPF, HPF, BPF and BSF using windowing technique
5. (a) Design of Butterworth Filter using Impulse Invariant and Bilinear transformation
   (b) Design of Chebyshev Filter using Impulse Invariant and Bilinear transformation
6. (a) Implementation of Decimation and Interpolation Process.
   (b) Implementation of I/D sampling rate converters.
7. (a) Study of TMS320C54X DSP processor
   (b) Arithmetic operation using TMS320C54XX
8. MAC operation using various addressing modes
9. (a) Linear Convolution
   (b) Circular Convolution
10. (a) FFT Implementation
    (b) Waveform Generation – Sine wave and Square wave
11. Implementation of FIR filter on DSP processor
12. Implementation of IIR filter on DSP processor

Suggested Readings:

1. Digital Signal Processing Using. **MATLAB**, Third Edition. Vinay K. Ingle and John G. **Proakis**

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B. Tech. (ECE) VI SEMESTER

PC3215ECELECTRONIC DESIGN AND AUTOMATION LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 25 Marks *SEE: 50 Marks*

List of Experiments:

Part A (Digital VLSI front-end Design)

1. Develop VERILOG HDL code and Test bench for the following:
   a. Multiplexer, Decoder, Encoder, Parity Generator, D flip-flop, four-bit adder and magnitude comparator using structural modelling
   b. Four-bit parallel adder/subtractor, zero/one detector and JK flip-flop using data flow modelling
   c. Arithmetic and logic unit, D, SR and JK flip-flops with synchronous and asynchronous resets, universal shift register and BCD- seven segment decoder using behavioral modelling
   d. Asynchronous, Synchronous, Ring and Johnson counters.
   e. Sequence Detector using Mealy and Moore type state machines.
2. Develop VERILOG HDL code for eight to three priority encoders using structural modelling and develop a test bench to cover all the functionalities. Assume each gate has a zero delay and three-simulation units delay.
3. Develop VERILOG HDL code for a four-bit carry look-ahead adder in structural modelling. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.
4. Develop VERILOG HDL code for four to sixteen decoder using two-to-four decoders and other combinational logic. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.
5. Using conditional operator, write Verilog HDL code to shift input *data* right arithmetic by the number of positions specified by another input *shift*. Develop test bench to cover all the functionalities.
6. Write Verilog HDL code to realize all bit Zero/One detector. Develop test bench to cover all the functionalities.
7. Develop Verilog HDL code to realize a MOD-10 synchronous decimal up counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
8. Develop VERILOG HDL code for the state machine of control unit of GCD processor.
9. Develop Verilog HDL code to realize a four-bit universal shift register. Develop test bench to cover all the functionalities.
10. Develop Verilog HDL code to realize a four-bit ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
11. Develop Verilog HDL code to realize a four-bit twisted ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
12. Design a clock generator where its output *clk* is initialized to 0 and has a period of 500-time units and a duty cycle of 70 %.

13. Design four-bit binary to Gray converter and Gray to binary converter.

14. Acquaint with Synthesis and FPGA porting of the code.

Part B (Digital VLSI back-end Design)

1. Design and analyze the following CMOS circuits:
    a. Inverter using static, ratioed, dynamic and domino logic styles
    b. Two-input NAND gate
    c. Two-input NOR gate
    d. Two-to-one Multiplexer using transmission gate
    e. Design a one-bit full adder circuit
    f. Design a one-bit SRAM cell.
2. Draw the layout and evaluate the performance of CMOS Inverter and two-input CMOS NAND gate.

Suggested Readings:

1. Samir Palnitkar, "*Verilog HDL A Guide to Digital Design and Synthesis,*" 2nd Edition, Pearson Education, 2006.
2. Ming-Bo Lin, "Digital System Designs and Practices: Using Verilog HDL and FPGA," Wiley India Edition, 2008.
3. John P.Uyemura "Introduction to VLSI Circuits and Systems" John Wiley & Sons, ISBN No: 9971-51-417-6, 2002.
4. Neil H E Weste and David Money Harris, "CMOS VLSI design: A circuits and systems perspective" 4th Edition, Pearson, 2015.

Faculty of Engineering & Technology
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Department of Electronics & Communication Engineering

B. Tech. (ECE) VI SEMESTER

PW3216EC SUMMER INTERNSHIP

Credits: 0

Instruction: 6 weeks *Duration of SEE: --*
CIE: 50 *SEE: ---*

Summer Internship is introduced as part of the curricula for encouraging students to work on problems of interest to industries. A batch of two or three students will be attached to a person from an Electronics Industry / R & D Organization / National Laboratory for a period of 8 weeks. This will be during the summer vacation following the completion of the VI semester course. One faculty member will act as an internal guide for each batch to monitor the progress and interacts with the Industry guide.

After the completion of the project, students will submit a brief technical report on the project executed and present the work through a seminar talk to be organized by the department. Award of sessionalsare to be based on the performance of the student at the work place to be judged by industry guide and internal guide (25 Marks) followed by presentation before the committee constituted by the department (25 Marks). One faculty member will coordinate the overall activity of Summer Internship.

Annexure

- ✓ Students should not choose same department subject as an Open elective subject.
- ✓ Students can select any one of the following subjects as an Open elective subject.

Open Elective subjects offered from different department

Sl.No	Course Code	Name of the subject	Branch
1	OE3213EC	Microprocessor and Interfacing	ECE
2	OE3207CS	Fundamentals of Data Structures	CSE

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B. Tech. (ECE) VI SEMESTER

OPEN ELECTIVE-I

OE3213EC MICROPROCESSORS AND INTERFACING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT I
Evolution of microprocessors, 8085 microprocessor architecture, addressing modes and instruction sets. Basic assembly language programming, pin configuration, timing diagram of read and write operation.

UNIT II
8086 architecture-functional block diagram, register organization, memory segmentation, programming model, pins description in maximum mode and minimum mode, timing diagrams.

UNIT III
Instruction formats, addressing modes, classification of instruction set, assembler directives, macros, 8086 microprocessor assembly language programs: simple programs involving data transfer operation, arithmetic operation, logical operation, branch operation, machine control operation, string manipulations, stack and subroutine operations.

UNIT IV
8255 Programmable peripheral interfaceblock diagram and various modes of operation. Interfacing of ADC, DAC, keyboard, seven segment display, stepper motor interfacing and 8254 (8253) programmable interval timers.

UNIT V
Interrupt structure of 8086, interfacing programmable interrupt controller 8259 and DMA Controller 8257 to 8086 microprocessor. Serial communication standards, RS 232,Serial data transfer schemes and block diagram of 8251 USART.

Suggested Readings:
1. Ramesh Gaonkar, "Microprocessor architecture, programming and applications with the 8085",Penram International Publication (India) Pvt. Ltd.
2. Douglas V. Hall, "Microprocessors and Interfacing", Tata McGraw Hill Publication.
3. Sivarama P. Dandamudi, "Introduction to Assembly Language Programing From 8086 to Pentium Processors", Springer Publication.
4. Walter A. Triebel and Avtar Singh, "The 8088 and 8086 Microprocessors: Programming, Interfacing Software, Hardware and Applications", Pearson Publication.
5. A. K. Ray and K. M. Bhurchandi, "Advance microprocessors and Peripherals" Tata McGraw Hill Publication.
6. Lyla B. Das, "The X86 Microprocessors, Architecture, Programming and Interfacing (8086 to Pentium)", Pearson Publication.

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B. Tech. (ECE) VI SEMESTER

OPEN ELECTIVE – I

OE3207CS FUNDAMENTALS OF DATA STRUCTURES

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT-I

Introduction: Introduction to data structure, types of data structures, revision of arrays, memory representation of arrays, operations on arrays, static versus dynamic memory allocation, pointers, self-referential Structure Time complexity.

UNIT-II

Stack-Queue (Linear Data structures): Definition of stack, operations on stack, implementation of stack. Applications of Stack.

UNIT-III

Definition of queue, operations on queue, implementation of queue using arrays
Applications of queue, Circular queue and priority queue.

UNIT-IV

Trees-Graphs (Nonlinear Data structures): definition of trees, Terminology on trees, binary tree, binary search tree and its operations, tree traversal techniques. Applications of Trees.

UNIT-V

Graph: definition, terminology on graphs, representation of graphs, graph traversal techniques, spanning tree, minimum cost spanning tree algorithms. Applications of Graphs.

Text Books:

1.Sahni Horowitz, “Fundamentals of data structures in C”, UniversitiesPress, second edition, 2008, ISBN No- 978-8173716058.
2.R Venkatesan,S Lovelyn Rose,“Data structures”,Wiley, second edition, 2019, ISBN No-978-8126577149.

References:

1.Narasimha Karumanchi, “Data Structures and Algorithms Made Easy: Data Structures and Algorithmic Puzzles”, Careermonk Publications, 2016, ISBN-No: 978-8193245279.

ABBREVIATIONS

L	:	Lectures	T	:	Tutorials
P	:	Practicals	CIE	:	Continuous Internal Evaluation
SEE	:	Semester End Examination	PC	:	Professional Core
OE	:	Open Elective	PW	:	Project Work

**Students have to undergo summer internship of 6 Weeks duration at the end of semester VI and valuation will be done in VII semester.